CLAIM AMENDMENTS

1. (previously amended) An on-chip differential multiple layer inductor comprises:

a first node on a first layer of a plurality of metal layers of an integrated circuit;

a second node on the first layer; and

a multi-layer winding on at least some of the plurality of metal layers, wherein the multi-layer winding is coupled to the first and second nodes, wherein the multi-layer winding is symmetrical with respect to the first and second nodes, and wherein metallization of the winding on each of the at least some of the plurality of metal layers is in an approximate range of twenty to eighty percent.

2. (previously amended) The on-chip differential multiple layer inductor of claim 1, wherein the multi-layer winding comprises:

first partial winding on at least one of the at least some of the plurality of metal layers; and

second partial winding on at least another one of the at least some of the plurality of metal layers, wherein positioning of the second partial winding with respect to positioning of the first partial winding establishes a parasitic capacitance that, in combination with inductance of the on-chip differential multiple layer inductor, provides a resonant frequency of approximately twice an

operating frequency of the on-chip differential multiple layer inductor.

3. (previously amended) The on-chip differential multiple layer inductor of claim 2, wherein the multi-layer winding comprises:

the at least one of the at least some of the plurality of metal layers is an adjacent metal layer to the at least another one of the at least some of the plurality of metal layers, wherein the positioning of the first partial winding is offset from the positioning of the second partial winding.

4. (previously amended) The on-chip differential multiple layer inductor of claim 2, wherein the multi-layer winding comprises:

an unused metal layer of the plurality of the metal layers, wherein the unused metal layer is between the at least one of the at least some of the plurality of metal layers and the at least another one of the at least some of the plurality of metal layers, wherein the positioning of the first partial winding is aligned with the positioning of the second partial winding.

5. (currently amended) The on-chip differential multiple layer inductor of claim 1, wherein the plurality of metal layers ~~further~~ comprises:

a plurality of thicknesses , wherein the at least some of the plurality of metal layers have a greater thickness of

the plurality of thicknesses than other metal layers of the plurality of metal layers ~~including thicker metallization layers~~.

6. (previously added - original) The on-chip differential multiple layer inductor of claim 1 further comprises:

a center tap coupled to the multi-layer winding such that the multi-layer winding is symmetrical about the center tap with respect to the first and second nodes.